Code: EC4T3

II B.Tech - II Semester - Regular Examinations - JUNE 2015

SWITCHING THEORY AND LOGIC DESIGN (ELECTRONICS AND COMMUNICATION ENGINEERING)

Duration: 3 hours Marks: 5x14=70

Answer any FIVE questions. All questions carry equal marks

- 1. a) Determine the value of base if $(193)_x=(623)_8$ 4 M
 - b) Convert (F4D2)₁₆ into Decimal. 3 M
 - c) The message below was coded in the Hamming code and transmitted through a noisy channel. Decode the message assuming that a single error has occurred in each code word: 10110110111100111000111010111. 7 M
- 2. a) Explain the importance of Boolean algebra in digital system.

 3 M
 - b) For the function given below 7 M $F=ABC+B\overline{C} D+AB\overline{C}$
 - i) Express F in standard form.
 - ii) Realize F using NAND gates only.
 - c) Simplify the expression $Y(A,B,C)=(A+B)(A+B+C)\overline{C}$ 4 M

- 3. a) A system has four inputs. The first two inputs a, b represent a number in the range 1 to 3(0 is not used). The other two inputs c, d represent a second number in the same range of 1 to 3(0 is not used). The output 'f' is to be '1' if the two inputs differ by '1' or more than '1'. Derive the truth table and minimal SOP expression using K-map.

 7 M
 - b) Simplify the following five variable Boolean expression using Quine McCluskey method. 7 M $F=\sum (0,1,9,15,24,29,30)+d(8,11,31)$
- 4. a) Design BCD to Excess-3 code converter using truth table,K-maps and logic circuits.
 - b) Implement a full subtractor using two 4:1 multiplexers. 7 M
- 5. a) Realize the following equations with a suitable PLA. Draw the logic diagram using PLA.

 7 M $F_1(A,B,C,D)=A\overline{B}D+A\overline{A}B\overline{D}$, $F_2(A,B,C,D)=A+B\overline{D}$
 - b) Realize the following functions using PAL and draw the logic diagram using PAL.

 7 M

$$F(A,B,C) = \sum m(3,4,5,7)$$

$$G(A,B,C) = \sum m(1,3,5,6,7)$$

$$H(A,B,C) = \sum m(1,4,5)$$

- 6. a) Design a conversion logic to convert SR flip flop to JK flip flop.

 7 M
 - b) Design a synchronous counter with the following binary sequence 0,4,2,1,6 and repeat. Avoid lockout condition and use D flip flops.

 7 M
- 7. a) Design a sequential circuit with two D FFs A and B and one input x. When x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats.

 7 M
 - b) Convert the following mealy machine into a corresponding Moore machine.

 7 M

PS	NS,Z	
	X=0	X=1
Α	B,0	E,0
В	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

8. a) Design an asynchronous sequential circuit with two input, I₁ and I₂ and one output Z. Initially both inputs are equal to zero. When I₁ or I₂ becomes 1, Z becomes 1. When the second input goes to 1, the output changes from 1 to 0. The output says at 0 until the circuit goes back to (0,0). 7 M

b) Realize the following switching function by a hazard free logic gate network.

$$T(x,y,z) = \sum (0,2,4,5)$$

7 M